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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

TRAN, DENISE

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 06/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

TD

Office Action Summary

Application No.

08/890,894

Applicant(s)

CHAUVEL ET AL. 

Examiner

Denise Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 March 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-15, 17, 19 and 34-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19 is/are allowed.
- 6) ☐ Claim(s) 6-15, 17 and 34-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 07/902,191.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

1. The applicant's amendment filed 3-28-02 has been considered. Claims 1-5, 16, 18, and 20-33 have been canceled. Claims 6-15, 17, 19, and 34-39 are presented for examination.

2. Claims 36-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Finch et al., US Patent No. 4783778, hereinafter Finch.

As per claims 36-39, Finch teaches the invention as claimed, an apparatus comprising: a first processor or a protocol processor (e.g., fig.1, B processor) where the first processor being suited to execute tasks to which a main processor is not suited (e.g., B processor performing x.25 protocol processing, col. 14, line 48 and A processor controlling mini packet protocol, Netlink protocols, initialization, col. 8, line 31 and et seq.), comprising a core (e.g., fig.1, el. 65sc102), a program memory (e.g., col. 14, line 22 and et seq. or col. 8, line 38 and et seq.), and a local memory (e.g., fig. 1, buffer of B processor or col. 6, line 62 and et seq.); a second processor or the main processor (e.g., fig.1, A processor; and col.8, line 36 and et seq.), where the second processor, of a design other than the first processor (e.g., fig. 1, A processor comprising: ROM and mini packet receiver/ transmitter (MPRT), of a design other than B processor having protocol serial controller (MPSC) and baud rate generation circuit), comprising a core (e.g., fig.1, el. 65sc102), a program memory (e.g., fig.1, ROM), and a local memory (e.g., fig.1, RAM of A processor); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, col. 8, line 55 and et seq., or

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fig.1, el. common memory interface and control); and one and only one common memory coupling the local memory of the first processor to the local memory of the second processor (e.g., fig.1, common memory).

3. Claims 6-7, 9-15, 17 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (hereinafter Aoyama) in view of Asano et al., U.S. Patent No. 5237686, (hereinafter Asano). The rejections are maintained set forth in the previous Office action.

As per claims 6 and 36, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig.1, el. 600), comprising a core (e.g., fig.1, el. 601); a second processor for performing vector processing, of a design other than the first processor (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory circuit for coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second

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processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

As per claims 7, Aoyama shows the use of the second processor being a main processor (e.g., col.4, line 63 and et seq.).

As per claim 9, Aoyama does not specifically show the second processor as a DSP. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality.

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As per claims 10-13, Aoyama does not specifically show the local memories as RAM; the program memory as a ROM. Asano (e.g., figs. 1-2, els 22, 17; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of having a local memory as RAM and a program memory for each processor are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the system of Aoyama because it would allow a storage location to be read and written in any order by having local RAM and increase processing speed of each processor by having local RAM memories and program memories, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show a program memory as a ROM. □Official Notice□ is taken that both the concept and advantages of providing; a program memory as ROM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include ROMs into the system of Aoyama because it would allow a storage system not to loose data when power is removed from it.

As per claim 14, 15, and 17, Aoyama teaches the memory circuit coupling between the first and second processors being physically separate from the first and second processors (e.g., fig.1, el. 800); the memory circuit being DPRAM memory (e.g., col. 10); and the synchronizing circuit ensure that only one of the processors utilized the memory circuit at any one time (e.g., cols. 5-6). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one

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and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

4. Claims 8 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of Morris Mano, Computer System architecture, 1982, pages 264 and 282-283, (hereinafter Mano).

As per claim 8, Aoyama does not specifically show the scalar processor as a microprocessor. Mano, page 264, line 8 and et seq., is cited merely as an example to show both the concept and advantages of providing a processor into a microprocessor are well known and expected in the art. It would have been obvious to one of ordinary

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skill in the art at the time the invention was made to include a processor into a microprocessor to Aoyama because it would provide for a reduction in space and signal lines between functional elements, leading to an increase in processing performance, and a low cost.

As per claim 35, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.) ; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of vector processing including signal processing tasks generally carrying out by a DSP and matrix computation performed by an array processor. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Mano, e.g., page 282 line 36 and et seq., has been cited as an example to show that both the concept and advantages of providing vector processing including the use of array processor for performing matrix computations are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include an array processor performing array computations into Aoyama because it would allow parallel computations on large arrays to be performed, thereby, increasing system computation power.

5. Claims 34-35 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of applicants admitted prior art, Background of the invention, the instant specification page 1 line 6 to page 2, line 11, (hereinafter AAPA).

As per claims 34-35, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.) ; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Also, AAPA, the instant specification, e.g., page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing scalar processing encompassed a high level task which is the

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monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing or a protocol processor; and vector processing including the use of array processor type are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing and an array processor performing array computations into Aoyama because it would allow protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality.

As per claims 37-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing of a design other than a main processor (e.g., fig.1, el. 600), comprising a core (e.g., fig.1, el. 601) where the first processor being suited to execute tasks to which a main processor is not suited; a second processor or the main processor (e.g., col.4, line 63 and et seq.), for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main

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storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. AAPA, the instant specification page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing because it would allow protocol processing to be performed; thereby, increasing system functionality.

6. Claims 34 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et

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al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of Finch et al., U.S. Patent No. 4783778, (hereinafter Finch).

As per claim 34, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els. 500 and 600 and cols. 2, line 5 and et seq.); and the scalar processor (e.g., fig. 1., els. 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing. Finch, e.g., col. 8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing or protocol processor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

As per claims 37-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor (e.g., fig.1, el. 600) for performing scalar processing, of a design other than a main processor or of a design which enables the processor to execute tasks, where the first processor being suited to execute tasks to which a main processor is not suited, comprising a core (e.g., fig.1, el. 601) ; a second processor or the main processor (e.g., col.4, line 63 and et seq.), for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second

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processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. Finch, e.g., col.8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing are well

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known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

7. Claim 19 is allowable over the prior of record.

8. Applicant's arguments filed 3-28-02 have been fully considered but they are not persuasive.

9. In the remarks, the applicant argued (1) that processor A and processor B are of the same design or suited to performed the same tasks.

As to point (1) the examiner disagreed with the applicant's arguments because Finch teaches the invention as claimed, an apparatus comprising: a first processor or a protocol processor (e.g., fig.1, B processor) where the first processor being suited to execute tasks to which a main processor is not suited (e.g., B processor performing x.25 protocol processing, col. 14, line 48 and A processor controlling mini packet protocol, Netlink protocols, initialization, col. 8, line 31 and et seq.), comprising a core (e.g., fig.1, el. 65sc102), a program memory (e.g., col. 14, line 22 and et seq. or col. 8, line 38 and et seq.), and a local memory (e.g., fig. 1, buffer of B processor or col. 6, line 62 and et seq.); a second processor or the main processor (e.g., fig.1, A processor; and col.8, line 36 and et seq.), where the second processor, of a design other than the first

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processor (e.g., fig. 1, A processor comprising: ROM and mini packet receiver/transmitter (MPRT), of a design other than B processor having protocol serial controller (MPSC) and baud rate generation circuit).

10. In the remarks, the applicant argued (2) that it would not have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Asano which discloses processors for vector processing into Aoyama which discloses one processor for scalar processing and one for vector processing. Also, answer to the response to Examiner 's rebuttal (12).

As to point (2) the examiner disagreed with the applicant's arguments because Aoyama teaches the use of controlling a plurality of processors to access a common memory (e.g., col. 5, lines 1-10), and Asano discloses the same subject matters (e.g., fig.6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61). It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor. In further discussion, the examiner would apply the teaching of Asano as discussed above to modify the Aoyama but would not physically combine the two systems together. Basically, the feature is very well known in any type

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of computer architecture field. The examiner is simply choosing one of many to use as an example, to show Applicant's claimed features. Even though Asano teaches vector processors and Aoyama teaches a vector processor and a scalar processor, both of the references teach controlling a plurality of processors for accessing a common memory. Therefore, the examiner would apply the teaching of each processor comprising ROM, a RAM (e.g., Asano, fig. 1, els 22-23) and one and only one common memory (e.g., Asano, fig.17 and 6, els. 62 , 172 and fig. 1, el. 14a coupling the processors to a common memory 1).

11. In the remarks, the applicant argued (3) that Applicants challenge the Examiner "it would increase processing speed of each processor by having ... for each processor" applicant's amendment filed 3/28/02 page 14.

As to point (3) in response to the applicant's arguments Shimoda (5210861) shows fig.1, the use of having data from a local cache 3A instead of having data from a common memory 7c every time to increase processing speed. Morris Mano, page 502, lines 13-14 teaching the use of a cache to increase speed processing of a processor.

12. In the remarks, the applicant argued (4) that Asano fails to teach or suggests a "synchronizing circuit for coupling the core of said first processor to the core of said second processor," claims 6 and 36. and the response to the examiner 's rebuttal (13)

As to point (4) the examiner disagreed with the applicant's arguments. In response to applicant's arguments against the references individually, one cannot show

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nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Even though the examiner used Aoyama to show the use of the synchronizing circuit (e.g., fig. 1, els. 810 or 800a, col. 5, lines 1-10), also, Asano clearly teaches or suggests a synchronizing circuit for coupling the core of said first processor to the core of said second processor (e.g., fig.6, el. 71 controlling the plurality processors to access a common memory 62; and col. 12, lines 58-61). It does not matter whether Asano teaches or does not teaches a synchronizing circuit for coupling the core of said first processor to the core of said second processor because Aoyama teaches the feature as stated in the rejection above.

In further discussion, with respect to claim 36, In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., synchronizing circuit for coupling **the core of** said first processor to **the core of** said second processor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

13. In the remarks, the applicant argued (5) that Asano discloses "multiple common memory but not "one and only one common memory coupling the local memory of the

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first processor to the local memory of the second processor.” Also, answer to response to examiner rebuttal (14).

As to point (5) the examiner disagreed with the applicant’s arguments. Asano clearly discloses one and only one common memory coupling the local memory of the first processor to the local memory of the second processor,” (e.g., fig.6, a common memory 62; and col. 12, lines 53-61; fig. 1, el. 14a coupling the processors to a common memory 1, or fig.6 and 17, els.62 , one and only one common memory 172 couple to local memories 174a-174b).

Also, in fig. 1, show at a specific time one and only one common memory of the memories being access(coupled) by a processor.

14. In the remarks, the applicant argued (6) Aoyama fail to teach or suggest wherein the second processor is the main processor of the apparatus.

As to point (4) the examiner disagreed with the applicant’s arguments. Aoyama teaches or suggests wherein the second processor is the main processor of the apparatus. For example, “the vector processing system,” col. 4, line 63. Because the vector processing is a main processing in the system, it is called the **vector processing system** but not a scalar- vector processing system or a scalar processing system; therefore, vector processor is a main processor of the vector processing system.

15. In the remarks, the applicant argued (7) Aoyama and Asano fail to teach or suggest wherein the second processor is a DSP.

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As to point (7) the examiner disagreed with the applicant's arguments. Asano (e.g., col. 1, line 16 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art.

16. In the remarks, the applicant argued (8) Aoyama and Asano fail to teach or suggest the use of RAM and ROM.

As to point (8) the examiner disagreed with the applicant's arguments. Asano (e.g., figs. 1-2, els. 22, 17; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of having a local memory as RAM and a program memory for each processor are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the system of Aoyama because it would allow a storage location to be read and written in any order by having local RAM and increase processing speed of each processor by having local RAM memories and program memories, thereby increasing the processing efficiency for each processor. Aoyama and Asano do not explicitly show a program memory as a ROM. Official Notice is taken that both the concept and advantages of providing a program memory as ROM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include ROMs into the system of Aoyama because it would allow a storage system not to lose data when power is removed.

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17. In the remarks, the applicant argued (9) Aoyama and Asano fail to teach or suggest wherein the memory circuit for coupling the local memory of the first to the local memory of the second processor being physically separate from the first and second processors.

As to point (9) the examiner disagreed with the applicant's arguments. Aoyama teaches the memory circuit for coupling the local buffer of the first processor to the local register of the second processor being physically separate from the first and second processors (e.g., fig.1, el. 800). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and

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program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

18. In the remarks, the applicant argued (10) Aoyama and Asano fail to teach or suggest wherein the memory circuit coupling the local memory of the first processor to the local memory of the second processor is a DPRAM memory

As to point (10) the examiner disagreed with the applicant's arguments. Aoyama teaches the memory circuit coupling the local buffer of the first processor to the local register of the second processor is a DPRAM memory (e.g., col. 10, line 15, RAM 108; and fig. 5, RAM 108 with dual ports. Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and

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program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Also, regarding to the applicant's response to Examiner's rebuttal (19), fig. 1, show a common memory 800a and fig. 5, shows a common memory **circuit** 108-1 as recited in claim 6.

19. In the remarks, the applicant argued (11) Aoyama and Asano fail to teach or suggest wherein the synchronizing circuit ensure that only one of the processors utilized the memory circuit for coupling the local memory of the first processor to the local memory of the second processor, at any one time (e.g., cols. 5-6).

As to point (11) the examiner disagreed with the applicant's arguments. Aoyama teaches wherein the synchronizing circuit ensure that only one of the processors utilized the memory circuit for coupling the local buffer of the first processor to the local register of the second processor, at any one time (e.g., col. 5, line 63 and et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious

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to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Also, regarding to response to Examiner's rebuttal (20), Aoyama (e.g., col. 5, lines 63 and et seq.) teaches the use of a flip flop circuits (a circuit that changes between two possible states when a pulse is receive at the input) indicating an access to the common memory base on a pulse or timing and the use of the test and lock processing where in light of the applicant's specification line 7, lines 35-36 teaches "signals TAS which are intended for synchronization".

20. In the remarks, the applicant argued (12) AAPA does nothing to overcome the above-identified deficiencies of the Aoyama and Asano, nor is there any teaching of the combination of AAPA with the teaching of Aoyama and Asano.

As to point (12) in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir.

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1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, AAPA, the instant specification, e.g., page 1 line 13 to line 18, teaches "scalar processing encompasses a high level task which is the monitoring of the application or the management of functioning and tasks which are generally carried out by hardwired logic or a processor which may be identified as protocol processing" or protocol processor well known in the art and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation power and functionality.

21. In the remarks, the applicant argued (13) that Aoyama and Asano fail to teach or suggest "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP or the use of array processor type".

As to point (13) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the use of scalar processing encompassed in a high level task which is the monitoring of an application or the management or functioning and tasks generally carried out by a DSP or the use of array processor type".) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

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22. In the remarks, the applicant argued (14) there is no teaching or suggestion in AAPA that it could be combined with the teaching of Aoyama and Asano.

As to point (14) in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the instant specification, e.g., page 1 line 13 to line 18, teaches "vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which required a more powerful structure than that of the DSP and which is generally of the 'array processor' type." The use of vector processing including an array processor type is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing and an array processor performing array computations into Aoyama because it would allow protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality.

23. In the remarks, the applicant argued (15) there is no teaching or suggestion in AAPA that it could be combined with the teaching of Aoyama and Asano.

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As to point (13) in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, In this case, AAPA, the instant specification, e.g., page 1 line 13 to line 18, teaches "scalar processing encompasses a high level task which is the monitoring of the application or the management of functioning and tasks which are generally carried out by hardwired logic or a processor which may be identified as protocol processing" or protocol processor well known in the art and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation power and functionality.

24. In the remarks, the applicant argued (16) there is no teaching or suggestion in Finch that it could be combined with the teaching of Aoyama and Asano.

As to point (16) in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so

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found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Finch, e.g., col.8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

25 In the remarks, the applicant argued (17) that the examiner has provided no evidence to support her determination (i.e., it would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation power and functionality).

As to point (17) the examiner disagrees. The examiner has provided evidence to support her determination. AAPA states that protocol processing is generally carried out by the use of a scalar processor, as shown above. Aoyama shows the use of a scalar processor. AAPA adds functionality to a scalar processor (i.e., the protocol processor performs protocol processing). Therefore the evidence is the reliance of the AAPA.

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26 In the remarks, the applicant argued (18) the three basic criteria must be met (i.e., suggestion or motivation to combine the references, reasonable expectation of success and must teach or suggest ALL the claim limitations).

As to point (16) the examiner disagrees for similar reasons as above. Basically, the examiner has already shown above the suggestion or motivation to combine the references and where the prior art teaches or suggests ALL the claim limitations. As per reasonable expectation of success, of course there is reasonable expectation of success. AAPA has already stated that scalar processors can perform the protocol processing.

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Tuesday and an alternated Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for Official communications, (703) 746-7240 for Non Official communications, and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Denise Tran

6/3/02


MATTHEW KIM
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